



## Product/Process Change Notice - PCN 18\_0109 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

**PCN Title:** AD9545 Data Sheet Specification Changes

**Publication Date:** 06-Sep-2018

**Effectivity Date:** 06-Sep-2018 *(the earliest date that a customer could expect to receive changed material)*

### Revision Description:

Initial Release

### Description Of Change:

Revision of the AD9545 Product Data Sheet from RevA to RevB.

The following summarizes the data sheet specification changes...

#### 1) System Clock Inputs, XOA and XOB table:

- 1a) The Slew Rate for Sinusoidal Input expands to two line items below.
- 1b) Functional, >6 V/us TYP.
- 1c) Operational, >31 V/us TYP (formerly 50 V/us MIN).

#### 2) Reference Inputs table:

- 2a) Differential Mode Slew Rate limit change; from 20 V/us MIN to >4.1 V/us TYP.
- 2b) Addition of DC-Coupled, LVDS-Compatible Mode Slew Rate line item; >1.2 V/us TYP.
- 2c) Addition of Single-Ended Mode Slew Rate, 1.2V CMOS line item; >8 V/us TYP.
- 2d) Addition of Single-Ended Mode Slew Rate, 1.8V CMOS line item; >8 V/us TYP.
- 2e) Addition of Single-Ended Mode Slew Rate, AC-Coupled line item; >8 V/us TYP.
- 2f) Reference Demodulator Carrier Frequency, Band 0, DC Balanced Modulation change; from 30 MHz MAX to 40 MHz MAX.
- 2g) Reference Demodulator Carrier Frequency, Band 0, Unbalanced Modulation change; from 45 MHz MAX to 60 MHz MAX.
- 2h) Reference Demodulator Carrier Frequency, Band 1, DC Balanced Modulation change; from 90 MHz MAX to 120 MHz MAX.
- 2i) Reference Demodulator Carrier Frequency, Band 1, Unbalanced Modulation change; from 135 MHz MAX to 180 MHz MAX.
- 2j) Reference Demodulator Duty Cycle; MIN limits modified to include influence of Band 0/1 selection.

#### 3) Distribution Clock Outputs table:

- 3a) Differential Mode; addition of Rise/Fall Time line items.
- 3b) Differential Mode; addition of Duty Cycle line items.
- 3c) Single-Ended Mode; addition of Rise/Fall Time line items.
- 3d) Single-Ended Mode; addition of Duty Cycle line items.

#### 4) Time Duration of Digital Functions table:

- 4a) Addition of "Time from Release of Power Down to Completion of System Clock PLL Calibration" line item.
- 4b) Addition of "Time from Release of Power Down to System Clock PLL Locked and Calibrated" line item.

#### 5) Holdover Specifications table:

- 5a) Relative Frequency Accuracy, Cascaded DPLL Operation limit change; from 0 ppb TYP to 0 ppb MAX.
- 5b) Addition of Relative Frequency Accuracy, Non-Cascaded DPLL Operation line item; <1 ppb TYP.

#### 6) Auxiliary Circuit Specifications table:

- 6a) Addition of Time to Digital Converters (TDCs), Non-Periodic Operation line items.
- 6b) Time to Digital Converters (TDCs), Periodic Operation, Time Stamp Jitter (RMS) expands to two line items below.
- 6c) Reference Input; 7 ps TYP, 21 ps MAX (formerly 20 ps TYP with no MAX specified).
- 6d) M-Pin Input; 9 ps TYP, 26 ps MAX.

#### 7) Logic Output Specifications (M0 to M6) table:

- 7a) Addition of Rise/Fall Time line items.

#### 8) Temperature Sensor Specifications table:

- 8a) Accuracy, Absolute line item changes to Accuracy, Absolute Die Temperature
- 8b) Accuracy, Relative line item changes to Accuracy, Relative Die Temperature.

- 9) Addition of new tables:
  - 9a) Operating Temperature
  - 9b) Reference-to-Reference Coupling
  - 9c) Reference-to-Mx Pin Input Timing Skew
  - 9d) Output-to-Output Timing Skew
  - 9e) Output Timing Skew Between Mx and OUTXY Pins
  - 9f) DPLL Propagation Delay
  - 9g) DPLL Propagation Delay Variation
  - 9h) Mx-to-Mx Pin Output Timing Skew
  
- 10) Absolute Maximum Ratings
  - 10a) Addition of Output Drivers line item.
  - 10b) Removal of Operating Temperature Range line item (moved to the new Operating Temperature table in the Specifications section).
  
- 11) Addition of new Typical Performance Characteristics plots:
  - 11a) Mx Pin Waveforms for Various Load Conditions
  - 11b) DPLL Delay Compensation Versus Temperature, Differential AC-Coupled Input Reference Mode
  - 11c) DPLL Delay Compensation Versus Temperature, 1.8V CMOS Input Reference Mode
  - 11d) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 50 ppb
  - 11d) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 4.6 ppm
  - 11d) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 100 ppm

**Reason For Change:**

The data sheet is in the process of revision to more thoroughly and accurately specify device performance and functionality.

**Impact of the change (positive or negative) on fit, form, function & reliability:**

The changes described above have no impact on fit, form or reliability of the device.

**Product Identification** *(this section will describe how to identify the changed material)*

N/A, no physical change to device.

**Summary of Supporting Information:**

No physical changes to the die; no qualification is required.

**Supporting Documents**      None

**For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.**

**Americas:**  
PCN\_Americas@analog.com

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**Appendix A - Affected ADI Models**

**Added Parts On This Revision - Product Family / Model Number (2)**

AD9545 / AD9545BCPZ

AD9545 / AD9545BCPZ-REEL7

**Appendix B - Revision History**

| <b>Rev</b> | <b>Publish Date</b> | <b>Effectivity Date</b> | <b>Rev Description</b> |
|------------|---------------------|-------------------------|------------------------|
| Rev. -     | 06-Sep-2018         | 06-Sep-2018             | Initial Release        |
|            |                     |                         |                        |

Analog Devices, Inc.

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